Specification document
for
Video and Control Electronic Unit

INSTRUMENTS RESEARCH & DEVELOPMENT ESTABLISHMENT

DEFENCE RESEARCH & DEVELOPMENT ORGANISATION

MINISTRY OF DEFENCE

RAIPUR ROAD, DEHRADUN-248008

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The Detail Specifications for Video and Control Electronics Unit given in this document may undergo minor changes during tender/DDR/CDR with mutual discussion between the firm and the IRDE.

In case of any clarifications, the vendor may contact the following:

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1. Introduction

IRDE, Dehradun is proposing to involve experienced, interested and competent Indian partners for the development of the Video and Control Electronics Unit (VCEU) for Electro-optical Payload. This document is intended for the prospective bidders to understand the work involved in the development of VCEU. It presents the system requirements and its specifications, interface requirements, requirements of qualification testing, development time frame and other terms.

2. Vendor Evaluation/Qualification Criteria

The firm are expected to provide their proposal with maximum possible details to enable the evaluation committee of experts to assess the technical and financial capabilities of the firm without any ambiguity. Techno-Commercial Evaluation Committee (TCEC) may visit the firm premises, if felt necessary, to assess its capabilities and/or the firm may be called to IRDE for a detailed presentation (by the firm) regarding their capabilities, experience, development approach and financial status. For details refer Part IV of RFP.

3. Functional Description of VCEU

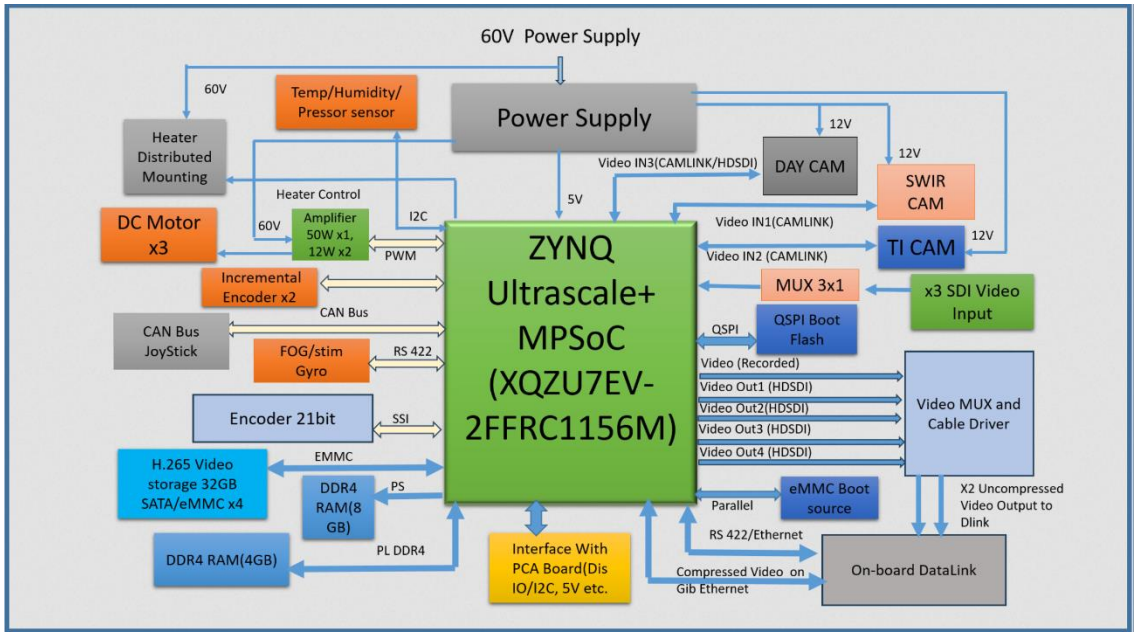
This document describes the specifications, firm's responsibilities and scope of work & deliverables for the development, realization and integration of VCEU for EO Payload.

Each Set of Video and Control Electronics Unit (VCEU) consists of the following items:

1. Processing Electronics Card – 01 No.
2. Power cum Amplifier Card - 01 No.
3. Interconnecting Cable Set with mating connectors - 01 set
4. Testing and software porting cables- 01 set
5. External Harnesses- 01 set
6. MWIR Sensor- 01 No
7. Day Sensor- 01 No
8. SWIR Sensor- 01 No

The two electronics cards mentioned above at S. No. 1 and 2 can be stacked or cabled as per fitment feasibility. The size and weight of each individual card will be

approximately 3”x3”x1”. The total weight of the two electronics cards should be approx. 300gms including connectors on PCB. Geometry (shape) of electronics cards is subject to change based on fitment in IRDE’s main housing under design. The Block diagram below (Fig.1) shows the overall electronics architecture.



(Figure 1: Architecture of Processing Electronics Card)

3.1 Processing Electronics Card (PEC)

The design of this card will be based on Zynq UltraScale + MPSoC (XQZU7EV-2FFRC1156M) host machine. This board will capture, process, record and display the multichannel videos. The entire video pipelines have to be implemented in block design using AXIS/VDMA/AXI Interconnect compliant components. This board has to provide the following interfaces and functions:

3.1.1 Input Video Interface

There will be 2 types of input video interfaces as discussed below-

a) **CAMLINK Input**

Three nos. of LVDS (04 pairs data and 01 clock) interface in LVDS bank of MPSoC configured to capture video format of 1280x1024P @30 frame per second from image sensors. There should be standard MDR(26 Pin) connectors to input video data, clock and configuration signals from detector output.

b) SDI (Serial Digital Interface) Input

One no. of HD-SDI input video interface to be implemented using GTX transceiver available in MPSoC. Input to GTX will come from 3 x1 video MUX. The MUX will receive 3 nos. of SDI video through miniature hybrid connector populated on board. Any one out of three videos should be selectable remotely to feed to MPSoC.

3.1.2 VCU (Video compression/decompression)

All three input videos on Camlink and one video on SDI should be routed to integrated Video Coder/Decoder Unit (VCU) in Zynq for H.265 compression. The Output of VCU should be recorded to on-board 32GB eMMC x4 chip which should be formatted as FAT32 file system for storage of all four video files.

Whenever required the recorded videos in eMMC chip should be decoded to stream out on one of SDI output interfaces for display. But at a time, any one out of three (user selectable) should be decompressed to stream out to SDI output port.

a) **Video Frames Buffers**

Video Frame Buffers of all four videos (03 CAMLINK and 01 SDI input) should be stored on DDR4 chips. Three video frames should be stored on PS DDR4(4GB). Frame should be accessible by software in PS for software processing. One video frames should be stored on PL–DDR4(2GB). The same should be accessible by PS for software processing.

b) Process Pipeline

Facility to process video by IP core-based filters for all four videos. Two process channels to be implemented in PS DDR4 and two in PL DDR4. There should be implementation of enable /disable for process pipeline so that whenever desired filters can be implemented in software or hardware. A standard convolution filter written in C/C++ to be synthesized in IP core filter and same to be used in process pipeline for demonstration purpose.

c) Output Video Interface

Five nos. of HDSDI output video interface should be implemented. On 3 HDSDI output port Camlink input video will be routed and fourth HD-SDI output port will

carry HDSDI input video, fifth HD-SDI output port videos will be routing decompressed video. Using 5x2 MUX just two video will go to the miniature hybrid connector via cable drivers. Video selection out of 5 to 2 should be user selectable.

d) **HDL Design**

All the PL implementation has to be done in block design based on AXI Lite, AXI4, AXIS based components using Vivado IP integrator.

e) **Petalinux Configuration /porting/OS based test App development**

A test application (Qt GUI /Command Line) to be developed to configure and test the overall application. Software support for configuring/accessing VCU, VDMA, EMMC, Ethernet, CAN, UART, File system for EMMC/SATA. Also demonstrate the writing of encoded bit-stream into mp4/mkv container files and store into eMMC or SATA SSD(chip based). The recording has to be done on two input video at a time continuously.

f) Ethernet 1Gbps Interface

This interface should be implemented for streaming in/out compressed video (mp4/mkv files) to standard device like PC/LAPTOP. Video here has to be played using standard video players like VLC. The interface may use RJ45 integrated connector on PCB for this. Use PS ETH1 for the same. RTC and IEEE1588 TSU to be enabled for time stamping on video frames.

g) Ethernet 10/100 mbps

One Ethernet of PS(ETH0) has to be used for command and monitoring to be terminated at miniaturized PCB mount Hybrid connector. Software upgradation should be possible on this interface by TFTP.

h) RS422/RS232

One RS422 and one RS232 interface to be implemented using PS UARTs. The signals to be terminated on PCB mount miniaturized Hybrid connector.

i) **Motor Interface**

There should be provision for driving one DC motor. For this a 50-watt H-Bridge IC (Populated in PCA Board discussed next) to be used to drive the motor. Integrated TTC peripheral of PS to be configured to generate PWM signal for controlling the duty of H-Bridge amplifier. Along with direction control, enable

disable signal and PWM signal and ground ref,4 pins to be allocated on miniature PCB mount connector for amplifier. Current and Voltage monitoring of motor power consumption to be also implemented. So here I2C signal also to be accounted for V & I monitoring. Proper Ground Isolation to be taken care.

j) **Motor (FOCUS) and Incremental Encoder Interface**

There should be provision for driving two 12W DC motors. For this a 12-watt H-Bridge IC with dual output (Populated in PCA Board discussed next) to be used to drive the motors. Interface logic to be implemented in PL to generate PWM signal for controlling the duty of H-Bridge amplifier and discrete control signals. Interface for two incremental encoders with (A & B) channels to be implemented in PL part. Along with direction control, enable disable signal, PWM signal, encoder supply, data signal and ground ref, 12 pins to be allocated on miniature PCB mount connector for amplifier. Current and Voltage monitoring of motor power consumption to be also implemented. So here I2C signal also to be accounted for V & I monitoring. Proper Ground Isolation to be taken care. Provision for two nos. of photo sensor interface for position reference is also required.

k) Gyro and Shaft Encoder Interface

Gyro interface on RS422 to be implemented to read the platform disturbances. SSI interface to be implemented in PL part for an absolute shaft encoder data reading. For this differential signal complying RS422 standard for CLK+, CLK-, DATA+, DATA- has to be implemented. For this 4 nos. pin at connector to be considered. Suitable encoder and gyro with similar interface may be used while implementation and testing.

l) **One RS422 Interface**

To be implemented with UARTLITE IP core. Signals and terminated at connector with RS422 transceiver.

m) **JOYSTICK interface**

CAN BUS based joystick interface to be terminated at miniaturized PCB mount hybrid connector. Signals includes CANH, CANL.

n) Discrete IOs Interface for Heater and DC-DC modules

Discrete signals (10 Output/ 6 Input) are required to operate DC-DC modules, power MOSFET used for driving Heaters, (Populated on PCA board).Isolation

provision has to be given for input as well as output. These signals will go to PCA board discussed next, via wired connection. Total 18 pins to be terminated on connector (16 discrete IO plus ground references). Apart from this heater current and voltage monitoring interface on I2C to be provided.

o) TPH interface

Temperature, pressure and humidity sensor interfaces on I2C Bus has to be implemented. Six temperature sensor PCBs (10x10mm) based on MCP808 temperature sensor IC have to be developed. The interface for all of them will be terminated on miniature hybrid connector which includes I2C clk and data & 3.3VH, 3.3VL. Total 24 pins are required for these 6 temperature PCB interfacing.

p) Heat Sink

Appropriate heatsink for Zynq FPGA chip has to be designed and thermal analysis has to be carried out.

3.2 Power cum Amplifier (PCA) Card

This card will be receiving input power at 60V to 100V from source and will generate various different supply using isolated PI series DC-DC modules from Vicor only. Description of all required output powers interfaces, control and monitoring interfaces, H-Bridge amplifier etc. has been given below.

1) 12V 2Amp (24W) peak power to be terminated at PCB mount miniature Hybrid connector.
2) 12V 3Amp (36W) peak power to be terminated at Hybrid connector.
3) 5V 3Amp supply to be generated using isolated converter for PEC board and any logic supply required on PCA board components.
4) Any (Discrete/RS422/I2C) interface going off-board either from PEC board or PCA board has to have isolated interface operated at isolated supply.
5) 48V 1Amp generation for H-Bridge amplifier. Output of amplifier will be terminated at PCB mount connector.
6) There will be input spike protection, polarity protection. Vicor recommended filter to be used for DC-DC modules.
7) I2C based current sensors has to be used for all 4 nos. of Heaters, Bridge amplifier, 12V DC-DC modules.

8) Control and monitoring interface between PEC and PCA card includes PWM control signal, enable, direction control, heater enable, DC-DC modules enable, I2C signals for current and voltage sensing.
9) The board will deploy the T-P-H sensor on it and I2C as configuration/monitoring interface with PEC card. If possible, for all I2C devices let there be one I2C port interface in PEC board.
10) The board will have two connectors one carrying all signal to PEC board and another connector carrying power signals and other to Heaters, amplifier, Power for EO payload i.e., 12V for three different devices, 5V for two nos. of servo sensor. Connector to be used should be 50 mil pitch metallic connectors.

4. Scope of Work

1) Development of Processing Electronics and Power cum Amplifier cards as mentioned in para 3 of this document.
2) Generation of schematics of both cards.
3) Design & fabrication of PCBs **(**MIL-Grade)
4) Procurement and population of electronics components.
5) Data Acquisition, Control interface and video processing for imaging sensors (MWIR, SWIR, Day):

a. Electronic Cards of VCEU will interface with the following sensors in their native resolutions with test optics:

A) Day Sensor
B) SWIR Sensor
C) MWIR Sensor

b. The VCEU's Electronic cards must be capable to offer compatibility with HD-SDI as well as LVDS Camlink inputs from the sensors simultaneously without affecting the framerate requirements.

c. The VCEU's Electronic cards should provide control and programmability of all the native features of the sensors (viz. Gain Manual/ AGC, AEC, thresholding and contrast enhancement, dark mode, low noise mode etc. based on OEM ICD and documentations). The unit should ensure readiness of transmission quality frames with traceable timestamping and GIS data from all the sensors.

d. The VCEU's Electronic cards should provide sufficient onboard memory to record reference dark frames @ various temperatures, store LUTs and video enhancement codes in Ultra RAM/Block RAM. Also, for permanent storage in eMMC/QSPI boot flash.

e. Porting of IRDE developed codes and implementation on real time video stream should be possible through command interface. Near real time performance should be ensured with desired latency of ≤ 2 frames. Further, latency to be discussed during development phase.

f. The unit should ensure noise free operation (Read noise < 2DN, DSNU < 2 DN & PRNU < 1%) and video buffers (if reqd) should be used along with filters.

g. Controls of the sensors to be provide through serial interface. All the OEM controls for the sensors and additional IRDE commands should be implemented. The command set should be accessible on-the-fly. Default mode operation controls to be identified and frozen in consultation with IRDE. The simultaneous command and control methodology should be implemented. Resource allocation to be done accordingly.

h. The unit should have EMI/EMC filtering inbuilt along with reverse polarity, high voltage, overload, transient and surge protection. Static protection should also be incorporated.

i. The thermal management plan of the unit should be comprehensive and incorporate the heat loads of various components.

j. The developer should ensure that requisite redundancies are maintained and single point failures identified.

k. VCEU electronic will also be used as the data acquisition and image processing of thermal imaging camera. The IR detector will be integrated with the VCEU electronics cards. From the IR detector LVDS Camlink data will be acquired by the VCEU electronics.

l. The electronics will require communication link for the IR Detector. VCEU electronic will provide the required power for IR Detector.

m. For the thermal imager image processing following process to be implemented:

1. Non uniformity calibration (NUC)

2. Bad pixel Replacement (BPR)
3. Automatic Gain Control (AGC)
4. Manual Gain Control (MGC)
5. Various image processing filter
6. Polarity change

n. The processed video from the VCEU electronics in HD-SDI format. There will be provision for selecting the video like TI, SWIR or Day Camera.

6) Electronics cards along with EO sensors after mounting on Test jig/housing will be tested as per para 5.1(e) of this document. Development of test jig/housing will be carried out by the firm as per IRDE inputs and interfaces of electronics cards and housing will be decided mutually.

7) Supply of MWIR, SWIR and Day Sensors as per Appendix A.

8) Assembly & Testing of PCBs.

9) Development of device drivers (BSP)/Porting Peta Linux, enabling Mali-400 integrated GPU, activating all four cortex a53 cores and two cortex R5 core.

10) Supply of Test cable for testing electronics.

11) Internal wiring/routing with one set of mating connectors per unit

12) External harness along with mating qualified small shell size 38999 connectors. One for power (60V 4Amp continuous) and one for communication (20 contacts). One Twin coax for video. (Per set). Other end of harness will deploy JSP series connectors. The Details will share during development phase.

13) Thermal design and analysis of each PCB for two extreme operating temperatures is required to be carried out and if necessary, design and fabrication of heat sink to be carried out.

14) Junction/case temperature of the electronic components should not exceed beyond their permissible operating limit and it should have safety margin of not less than 10°C and development of Heat Sink wherever required.

15) Orientation of the two boards with respect to gravity direction for thermal analysis will be conveyed by IRDE when required.

16) Temperature sensors are to be mounted on each board at two locations i.e., highest & lowest temperature locations.

17) Signal integrity test reports and de-rating analysis

18) Development of Test Software as per requirements of each card and overall functionality achievement.

19) Supply of all the BSPs and test application in source form.

20) Testing and functional acceptance as per para 5 of this document.

21) Technical Documentation (as per Section 6 of this document)

22) Technical and maintenance support during development and warranty period.

23) Joystick (APEM) with CAN bus interface (J1939).

24) Support during final integration, calibration and functional testing of electronics cards along with main system. The firm may require to depute their personal anywhere in India for this purpose and visit will be limited to 10 numbers.

25) Functional acceptance test procedure (document & ATP software) which will be prepared and has to be approved by IRDE. The document should be ready before boards are fabricated & populated. The test should cover all the functionalities implemented in both the boards (PEC & PCA card) as per section 3.1.3, 3.1.4, 3.1.5 above.

26) The acceptance test procedure for Environmental Testing and ESS as given in para 5.1 will prepared by the firm as per IRDE inputs and approved by IRDE.

5. Inspection and Acceptance Tests

Acceptance Criteria of VCEU is as follows:

5.1 Acceptance Criteria

The following acceptance criteria/standards should be adopted during hardware/firmware/software design. The firm to submit documents/test reports/Certificate to support that standard has been followed during development. IRDE & QA representative may visit during test.

a) MIL STD 275 for PCB design
b) MIL STD 31032 for bare PCBs
c) Screening tests qualification [As per Section 5.1.1]
d) *Environmental Stress Screening [MIL STD 2164]
e) Environmental Testing [As per Section 5.1.2]

VCEU electronics are required to undergo following tests and their test reports and documents to be furnished by the firm during the delivery.

*Designed for the test parameters, no test is required to be carried out.

5.1.1 Screening Tests qualification

1. The bare PCBs should qualify to MIL STD 31032
2. If all the Components populated are of MIL grade, then PCB screening mentioned below is not required.
3. If the bare PCB fabricated is of MIL Grade, and components (partially or fully) are of non-MIL grade then the populated PCB needs to undergo the screening mentioned below. The Populated PCBs should qualify to the Screening Test and a test report should be submitted to IRDE. The screening test will be done for all the deliverable PCBs. The Test parameters, details and requirements are tabulated below:

Visual Examination		
Title of Test	Test Details	Requirements
Visual Examination	Carry out Physical/Visual Examination of the assembled PCB for non-conformities / abnormalities and correct the same	As specified
	Performance Check/Functional Testing	As per ATP document
High Temperature Storage (Stabilization Bake) Test		
Title of Test	Test Details	Requirements

High Temperature Storage (Stabilization Bake) Test	As per test no. 22 of JSS 50101, after introduction of PCBs, increase the chamber temperature to +85˚C with tolerance +5˚C, expose the assembled PCB for 24 hours continuously at +85˚C (Off condition)	Visual Examination and functional checks at ambient temperature. Record failure observed if any.
Rework: Repair / Replace components as required using fresh components. The new components must undergo stabilization bake test before assembly.		
Thermal shock test: The PCB which has undergone the test of paragraph above shall be subjected to 10 cycles of continuous Thermal shock (in power OFF condition) as follows		
Test	Test Details	Requirements
Thermal Shock Test	As per Test Number 20 of JSS 50101: Low Temperature -40˚C with tolerance -5˚C High Temperature +85˚C with tolerance +5˚C Period of exposure: 30 minutes Transfer Time: 2 minutes No. of cycles: 10 Operation: Off Condition	PCB Assembly must be free from any visual damage or distortion namely • Cracking and de-lamination of finishes • Cracking and crazing of embedding and encapsulating compounds • opening of thermal seals and case seams • leakage of filling materials • Rupturing or cracking of hermetic seals and changes in electrical characteristics due to mechanical displacement or rupture of conductors or of insulating materials.
Visual Examination	On completion of 10 cycles, carryout visual examination using magnifying glass with magnification factor of 30 for detection of failures.	

Electrical measurements	Carryout performance checks as per mutually agreed ATP	As per ATP document
Acceptance criteria: In case of failure, analyses the defects in consultation with certification/quality assurance agency. Failed components shall be replaced and new components shall undergo stabilization bake and thermal shock before assembly. Repeat visual examination and performance checks.		
Burn-In test		
Title of Test	Test Details	Requirements
Burn-In Test	1. PCB shall be placed in a chamber. All arrangements shall be made externally to carry out Functional Checks on the PCB at every five hours period. This constitutes one cycle of five hours. 2. The temperature of the chamber shall be raised to +55˚C, the populated PCB is designed to perform with tolerance of +5˚C. 3. PCB shall be maintained at this temperature continuously for 48 hours in power ON condition. 4. In case of failure, the components shall be replaced by components which have undergone and passed high temperature storage and thermal shock before assembly and continue the test for remaining hours. If the failure occurs after the 46th / 47th / 48th hour, expose the PCB for further 03 hours to confirm the adequacy of the repair work. 5. On completion of burn-in test, switch off the chamber. 6. Take out the PCB assembly for conducting visual examination. PCB assembly shall be free from any visual damages or distortions as stipulated in 11.3.4 above. 7. Carry out the performance checks as per mutually agreed ATP on the PCB assembly and record the results.	The last three hours shall be defect free.
Marking: The assembled PCB on passing the above tests shall be marked suitable for easy identification to avoid mixing up of screened and unscreened PCBs.		

Post Burn-In: Subject the PCB assembly for complete performance checks, as per the respective test documents. If the PCB assembly can't be tested independently, insert it in the system/ test rig and check for the performance. Any non-conformity found during functional checks is to be recorded for further analysis and initiate appropriate corrective action.
Storage: Preserve the screened PCB assembly (duly marked for identification) in antistatic pouches safely and controlled environment for further integration with the equipment.
Record: Keep a record of all stage inspections and performance checks on the PCBs, identified with its serial number for later verification and traceability.

5.1.2 Environmental Testing

The following environment test will be conducted on VCEU electronics mounted in the test jig with sensors:

S. No.	Test	Standards/Remarks
1	Temperature	Without sensor: As per MIL STD-810H: Operating Temperature Range: -40°C to +55°C Storage Temperature Range: -55°C to +125°C
2	*Humidity	Conformal coating should be carried out
3	*Shock	2g, 24ms, Half sine- one shock per axis
4	*Vibration	MIL-STD-810G Method 514.6 ANNEX D, Category 13 (4grms)
5	*Electrostatic Discharge	DO-160G Section 25
6	*Voltage Spikes	DO-160G Section 17
7	EMI/EMC	DO-160G

*Designed for the test parameters, no test is required to be carried out.

6. Technical Documentation

S. No.	Documents
Hardware Documents	
1.	Hardware design document
2.	Schematics, PCB layouts, Gerber file
3.	Data sheets / reference manual of all components
4.	Acceptance Test Procedure of All Electronics Cards
5.	Acceptance Test Report of Electronics Card
6.	Bill Of Material
Software Documents required	
7.	Software Development plan
8.	PSAC Document
9.	Software requirement data
10.	Software Design Description
11.	Software Test Plan
12.	Software Test Description
13.	Software Test Report
14.	SW VDD
Hardware Analysis Reports	
15.	Thermal Analysis
16.	Reliability Analysis
17.	De-rating Analysis
18.	Signal Integrity Analysis
19.	EMI / EMC Analysis

20.	Screening Test Report for Populated PCB
21.	Environmental Test Reports

7. Deliverables:

Sr. No.	Item Description	Qty.
1	Processing Electronics Card	07 Nos
2	Power cum Amplifier Card	07 Nos
3	Interconnecting Cable Set with mating connectors	07 Sets
4	Testing and software porting cables	07 Sets
5	External Harnesses (Each set of 1-2m length with 38999 serial QPL certified mating connectors, 30 contact for signals, SMA for video, 4 contacts power connector at gimbal panel)	07 Sets
6	MWIR Sensor as per Appendix A	07 nos.
7	Day Sensor as per Appendix A	07 nos.
8	*SWIR Sensor as per Appendix A	06 nos.
*7th Set of VCEU will be delivered without SWIR sensor as given in the table above at Milestones mentioned in para 8.		

Accessories/Test kit (01 Set):		
1	Technical Documentation (as per list given in section 6) Hard and Soft Copy both	02 sets
2	Node Locked Vivado Design Suit Latest Edition Installed with SDKs (Vitis USP and Peta linux sdk) on portable test & development console with high end configuration.	02 Nos.
3	APEM Joystick	05 Nos.
4	Emulator for Zynq Ultrascale+ MPSoC (USB Platform Cable)	03 Nos.
5	Zynq Ultrascale+ MPSoC ZCU106 Development kit with FMC based accessories, LI-IMX274-MIPI-M12, FMC loop	02 Nos.

	back card and Teranex Mini HDMI to SDI & SDI to HDMI converter.	
6	Nodelock license for the following IP core- SATA 3.0 AHCI for Zynq Ultrascale + MPSoC HDMI2.0 TX/RX Subsystem	01 No.
7	Device drivers (with source codes) for processor (OS based & Bare metal both), license of all used IP cores and VHDL source codes for ATP applications of all required FPGA interfaces, block design files etc.	-

Note: The stages may incorporate modifications based on the feedback of trials and integration. One unit each of items mentioned at S. No. 1 to S. No. 4 under Accessories/Test kit to be essentially supplied along with Milestone delivery at T0+15 months.

8. Milestones with Acceptance Criteria

S. No.	Activity/Item description	Acceptance Criteria	Delivery period/Completion (Months)
1.	Detailed Design Review (See Note 1 below)	Acceptance by IRDE	T0+06
2.	1st and 2nd set of VCEU & Accessories/Test kit as mentioned in para 7	Compliance of Para 5.1 a, b, c & d and accepted by IRDE	T0+15
3.	Critical Design Review (See Note 2 below)	Acceptance by IRDE	T0+17
4.	3rd and 4th set of VCEU	Compliance of Para 5.1 a, b, c & d and accepted by IRDE	T0+24
5.	5th,6th and 7th set of VCEU & remaining Accessories/Test kit	Compliance of para 5 and accepted by IRDE	T0+36

Note 1: DDR: It should include but not restricted to:

- Detail Design for each functionality and interfaces
- Functional flow diagram
- BOM of each card
- Component layout
- Card size and mounting
- Power budgeting
- Heat load of each PCB
- Electrical ICD
- ATP

Note 2: CDR: It should include following but not restricted to:

- Signal Integrity, thermal and EMI/EMC analysis
- PCB Screening report
- De-rating and reliability analysis
- ATR

9. Warranty and Support

The firm to provide warrantee of 12 months. The warranty will start for all the deliverables under this contract after the final milestone (T0+36 months).

10. General Terms & Conditions

1) The firm should absorb minor changes/modifications without repercussions on cost.
2) Before submission of any document, the firm will send a draft copy of document for the necessary amendments/ corrections by IRDE. IRDE will hold the right to accept/ reject the document as per IRDE standards.
3) **All intellectual property rights (IPR) of the product will rest with IRDE**. The firm will not sell or modify the product or its variant to any party without written consent of the Director IRDE, Dehradun.
4) The firm should share the schematics with IRDE before launching the PCB fabrication.
5) All schematic, PCB Gerber data (complete PCB layout) will be handed over to IRDE as and when required during development.

6) A certificate to be furnished by the firm stating that Gerber files handed over to IRDE are the same by which PCBs supplied are fabricated. A certificate from the PCB manufacturer may also be enclosed for the same.
7) The Director, IRDE reserves the right to short-close the contract after any stage of part delivery if it does not meet the required performance or if the firm violates any of the technical or commercial terms and conditions.
8) Freight charges for any warranty replacement should be borne by the vendor.
9) Maintenance and technical support are required during development and warranty period.
10) The firm will provide product support for 05 years after warranty period.
11) The firm is responsible for ensuring the performance as per the specifications given in the development contract.
12) The firm must provide, in the techno-commercial bid, the development plan including micro-plan and number of engineers proposed to be employed on the project.
11. The firm must submit a compliance matrix with respect to all specification requirements and terms & conditions mentioned in this document for vetting by the TCEC. Vendor may be required to give a presentation before TCEC to enable the overall assessment of the vendor.
12. The firm should give its consent in the bid that the firm will depute project implementation team to IRDE for testing/inspection of hardware alongside IRDE team and attend reviews without additional cost implication whenever required.
13. The firm is liable to supply the item, developed under this contract to IRDE/IRDE designated agency, if required in future at reasonable cost.