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RESEARCH ARTICLE

X-Band 16-Channel Transmit-Receive Plank Unit for High-Resolution Imaging RADAR

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ABSTRACT This article presents a comprehensive design framework and realization approach for a state-of-the-art, X-band 16-channel Transmit-Receive (TR) plank unit for high-resolution imaging radar applications. The Transmit-Receive Module (TRM) is the most critical component of Active Electronically Scanned Arrays (AESA), which are widely used in Radar, Electronic Warfare (EW), and Communication systems. Modern AESAs with wide instantaneous bandwidth are utilized in imaging, and high data rate communication systems require time delay lines instead of narrowband phase shifters for squint-free beam scanning over a large scan volume. The design of a compact time delay line-based TRM that fits within the inter-element spacing of AESA is quite challenging. This paper presents a novel design of a true-time-delay (TTD) line-based 16-TR Channel (TRC) plank unit as a basic building block for X-band AESA-based high-resolution Imaging Radar. A novel architecture of distributed time delay network is proposed to offer a maximum time delay of 600 ps in steps of 3.125 ps per TRC by using 6-bit TTD line core chips at the plank unit level and overall 1.4ns maximum delay at AESA level. The proposed plank unit is realized by using a multi-layer, multi-laminate printed circuit board (PCB) technology with surface-mount microwave and digital components. Automated surface mount assembly and automated test facilities are utilized to develop plank units with high repeatability and reliability. The 16-TRC plank PCB is housed in a single mechanical enclosure along with blind mate connectors for RF, digital, and power supply interfaces. Two such plank units are mounted back to back on a single liquid cold plate for efficient thermal management. This paper details the design challenges associated with packaging and thermal management of multi-TR Channel plank units in a compact size of 300 $\times$ 200 x 8 mm^3 along with RF path analysis, circuit simulation, PCB design, and proto plank unit performance characterization. The designed plank unit has demonstrated 10 Watt peak transmit output power, receive noise figure of 4 dB per TRC, and channel-to-channel isolation of 40 dB over 2 GHz bandwidth.

INDEX TERMS Active electronically scanned array (AESA), complementary metal oxide (CMOS), commercially off-the-shelf (COTS), effective isotropic radiated power (EIRP), field programmable gate array (FPGA), gallium arsenide (GaAs), gallium nitride (GaN), low voltage differential signal (LVDS), monolithic microwave integrated circuit (MMIC), printed circuit board (PCB), single pole double throw (SPDT) switch, transmit-receive channel (TRC), true-time-delay (TTD) line.

I. INTRODUCTION

Active Electronically Scanned Arrays have found extensive applications in Radar, Electronic Warfare, and Communication systems. AESAs with immense capabilities like rapid beam agility, configurable power aperture, dynamic sidelobe level control, and beam shaping are indispensable in various domains [1], [2], [3], [4]. The TRMs distributed across the aperture of AESA play a pivotal role in attaining the required Effective Isotropic Radiated Power (EIRP)

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and sensitivity [5], [6], [7], [8], [9]. The TRMs are the critical component of AESA and constitute 40% to 50% of the size, weight and power (SWaP), and cost of an overall AESA-based system [10]. The multifunction AESA radars are widely used in defence applications, to perform tasks such as surveillance, tracking, and imaging [11], [12], [13]. The phased array radars for imaging and high data rate communication systems require large instantaneous bandwidth and suffer from beam squint and pulse stretching due to narrowband phase shifters employed for beam scanning [14], [15]. The wideband TTD lines, instead of narrowband phase shifters, offer squint-free beam steering over a wide instantaneous bandwidth and large scan volume for Radar, massive multiuser multiple-input multiple-output (MU-MIMO) systems, and wideband THz communication applications [16], [17], [18], [19], [20], [21], [22]. A typical X-band 10 cm resolution long-range imaging radar requires a time delay of a few nanoseconds for scan coverage of $\pm 60^0$ in both planes of AESA with 1000 elements [23]. The traditional TTD lines, such as Coaxial, Optical, or Planar transmission line types, offer longer time delays in the order of nanoseconds. However, they are bulky and lossy, imposing challenges to fit within the inter-element spacing of AESA [23], [24], [25]. The TTD lines in integrated circuit form are the most suitable components for integration at the TRM level; however, commercially available delay lines are limited to a maximum delay of 500 ps [26], [27], [28], [29], [30]. Recent advances in Microwave Photonic Integrated circuit delay lines are the most promising TTD line components for future wideband applications; however, they are currently in the research stage and commercially unavailable [31], [32].

In the past, various multi-channel TRM designs using TTD lines have been reported for wideband AESAs [33], [34], [35], [36], [37], [38], [39], [40]. Liu et al. presented a design of an 8-channel TTD line-based TRM in the Ku band over 1.2 GHz bandwidth using a low-temperature co-fired ceramic substrate (LTCC) with integrated phase shifters and TTD line MMICs [33]. Liu et al. introduced an 8-channel X-band TRM as a leadless system-in-package (SIP) in 3D configuration, integrating phase shifters and Complementary Metal Oxide (CMOS) TTD line integrated circuits (ICs) [34]. The hybrid configuration of integrating phase shifters at the TRM level and TTD line circuits at the sub-array level increases complexity and performance limitation due to array quantization sidelobes [35], [36]. Sreenivasulu et al. reported a 4-channel TRM design using a commercially off-the-shelf (COTS) 6-bit TTD line core chip of 200 ps max delay and GaN power amplifier to deliver 4W output power per channel [37] for small-size AESA. Additionally, they designed a wideband octal TRM for a 32-element EW phased array employing narrowband switched phase shifters over a 1-6 GHz frequency in a time-shared manner [38], which had the limitation of covering the full band in a single sweep. Han et al. reported the design of eight channel power division time delay module for 635 ps maximum time delay designed using one GaAs 6-bit TTD chip (315 ps) and 1-bit TTD (320 ps) MMICs with low output power of 5 dBm over 6-18 GHz as hybrid integrated circuit to feed 8 TR modules [39]. Sreenivasulu et al. reported the design of an Octal TRM using a commercially off-the-shelf (COTS) 7-bit TTD line core chip of 508 ps max delay and GaN power amplifier to deliver 8W CW output power per channel over 1-6 GHz for EW application to cover complete band in a single sweep instead of switched phase shifters [40].

This paper details the architectural design of a 10 cm resolution X-band (8.5-10.5GHz) 512-element AESA imaging radar by using a 16-TRC plank unit as a basic building. It presents an innovative approach to achieve a 1.4ns maximum time delay required to cover a large scan volume of AESA through a distributed time delay network integrated at plank unit and quadrant RF beamformer level. The paper discusses design challenges associated with packaging and thermal management of multi-TRC plank in a compact size of 300×200 x 8 mm^3. The designed plank unit delivers 10 Watt peak transmit output power, receive noise figure of 4 dB per TR channel, and channel-to-channel isolation of 40 dB over 2 GHz bandwidth. The paper is organized into six sections: Architectural design of time delay steered high-resolution imaging radar is covered in Section II. The plank unit's architectural, PCB, and mechanical designs are covered in Sections III and IV. The performance characterization of the prototype plank unit is described in Section V, and the conclusions in Section VI.

II. TIME DELAY STEERED HIGH-RESOLUTION IMAGING RADAR

AESAs for high-resolution imaging radars with wide instantaneous bandwidth (IBW) exceeding 1GHz employ a differential time delay between array elements to overcome the issues of beam squint and pulse stretching due to narrowband phase shifters used in conventional phased array radars [41], [42]. The TTD line is the key component of time-steered AESAs, which offers frequency-independent time delay over a wide IBW. Delay lines are either switched transmission lines of different lengths or LC circuits to provide a time delay proportional to the length (l) of the line, which is independent of frequency. In the case of time delay steering, progressive time delay (τ_d) across the array cannot be wrapped; hence, large time delay of the order of a few nanoseconds is required for large-size AESAs to steer the beam over comprehensive scan volume. A novel architecture of an X-band 512 (16×32) element AESA for 10 cm high-resolution imaging radar of 40 Km slant range is designed based on a distributed time delay network architecture to cover scan volume of $\pm 45^0$ in azimuth and $\pm 30^0$ in elevation planes. The designed array configuration, as shown in Fig. 1, utilizes 32 numbers of 16-TRC plank units (512-TRCs) along with 512 wideband cavity-backed slot

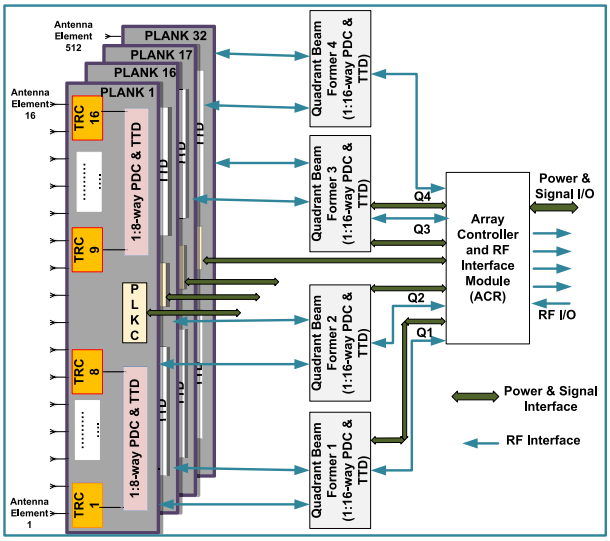

FIGURE 1. Block diagram of a TTD line-based 512-element active electronically scanned array.

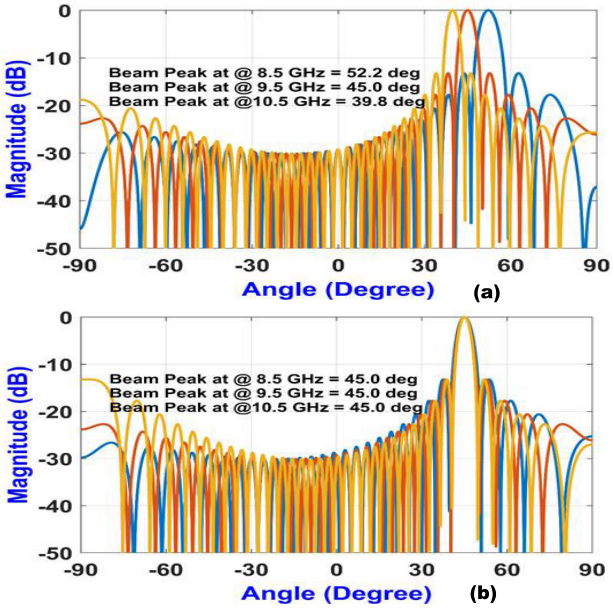

FIGURE 2. The simulated Antenna pattern of X-band 512 element AESA over 2 GHz bandwidth steered to azimuth angle of 45^0 (a) with phase shifters, and (b) with TTD lines.

antenna elements [43], quadrant beam formers, RF interface modules, and an array controller. As a line replaceable unit of AESA, the plank unit integrates multiple 6-bit TTD line MMICs and constitutes a distributed time delay network. In order to achieve 10 cm resolution for X-band 512 element AESA radar (IBW of 1.2 GHz), a time delay of 1.3ns is required for squint-free beam scanning of $\pm 45^0$ in azimuth (θ) and $\pm 30^0$ in elevation (ϕ) as per Equations (1) and (2) below [23].

$$\text{Time delay}(\tau_d) = m \times \tau_x + n \times \tau_y \tag{1}$$

$$\tau_x = \frac{d_x \sin(\theta)\cos(\phi)}{c}, \ \tau_y = \frac{d_y \sin(\theta)\sin(\phi)}{c} \tag{2}$$

where τ_x and τ_y are progressive time delays, m=16 and n=32 are a number of antenna elements, d_x=d_y=16 mm is the inter-element spacing in the X and Y-axis, respectively, c is the velocity of light in free space. The simulated antenna pattern of AESA steered to an azimuth angle of 45^0 by using phase shifters and TTD lines is shown in Fig. 2(a) and Fig. 2(b), respectively, over 2 GHz bandwidth, which depicts beam squint is more than $\pm 7^0$ (beam shifts on both sides of center frequency from desired steering angle) with phase steering and without any beam squint using time delay steering.

This design employs a novel distributed True Time Delay (TTD) line network to achieve a 1.4ns maximum time delay for the required scan coverage by implementing 600 ps at plank unit level and 800 ps at quadrant RF beamformer level, including 100 ps for TRC error compensation. At both levels, the time delay network uses a wideband COTS 6-bit TTD line core chip (RFCORE RMF040160P). The TTD line core chip is integrated at each TRC level, offering a finer resolution of 3.125 ps and a maximum delay of 192 ps. The core chip is selected to meet the maximum time delay requirement of the array to cover scan volume and resolution to achieve sidelobe levels better than 25 dB in receive mode [23]. The design details of the sub-functional blocks of the 16-TRC plank unit are presented in the sections below.

III. DESIGN TOPOLOGY OF 16-TR CHANNEL PLANK UNIT

The X-band 16-TRC plank unit is the critical Line Replaceable Unit (LRU) configured to provide the required time delay steering, transmit output power, low noise amplification, and side lobe level control in the receive mode of the AESA radar system. In plank/brick architecture [10], the TRCs are interfaced perpendicular to the array plane, offering more circuit space for integrating a distributed time delay network and better thermal management than the Tile architecture. The tile architecture integrates multiple TR modules with associated radiating elements, RF, control, and power distribution networks on a single multi-layer PCB within the inter-element spacing by using highly integrated multi-channel beamformer and front-end TR chips [44], [45], [46], [47], [48]. The design of tile-based TR modules is quite complex and challenging in terms of thermal management. Since multi-channel TTD core chips are not available commercially, plank-based architecture is chosen for the proposed design. The functional block diagram of the designed plank unit, as shown in Fig. 3, seamlessly integrates 16-TRCs, four 1:4-way power divider/combiners (PDC) equipped with dual TTD line circuits, two 1:2-way PDCs, a plank controller, and power supply circuitry as a unified entity. Each TRC features a 6-bit TTD line core chip, a Gallium Nitride (GaN) power amplifier, a circulator, Gallium Arsenide (GaAs) gain amplifiers, and low-power SPDT switches. The Field Programmable Gate

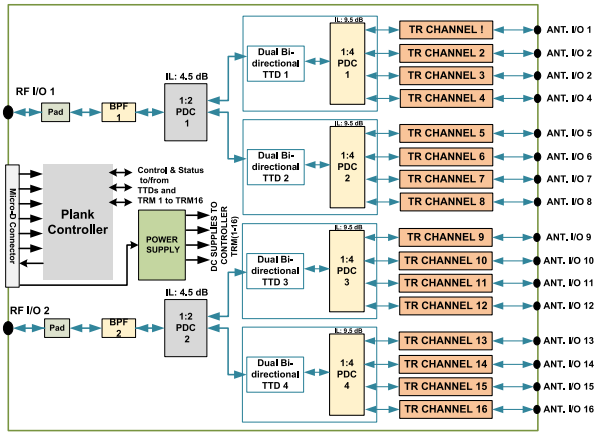

FIGURE 3. Functional block diagram of 16-TR Channel Plank Unit.

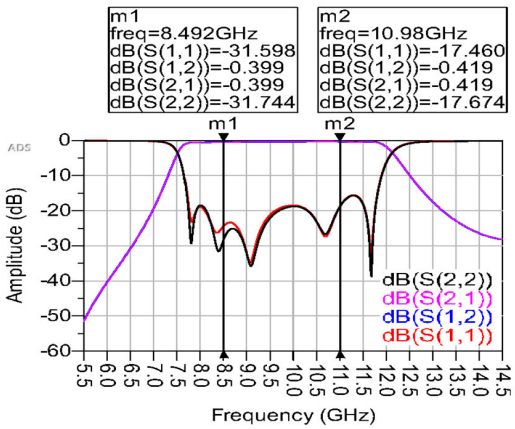

FIGURE 4. Simulated S parameters of Bandpass filter.

Array (FPGA) based plank controller generates the requisite control and timing signals, monitors the health status of all 16 TRCs, and reports to the system controller. The power supply circuitry generates the necessary low DC supply voltages for all TRCs and FPGA controller. A five-section X-band microstrip bandpass filter (BPF) of 2 GHz bandwidth is designed and simulated using the Pathwave Advanced Design System (ADS) tool from Keysight. The simulated Scattering parameters of BPF in Fig. 4 show insertion loss $\leqslant -1$ dB over 2 GHz bandwidth. Two numbers of BPFs are integrated, each common to 8 TRCs. The 16-TRCs, along with the controller, PDCs, and power supply circuitry, are meticulously integrated into a single multi-layer PCB housed within a compact mechanical enclosure. The plank unit is blind-mate interfaced with radiating elements without RF cables. For efficient heat dissipation, such two plank units are securely mounted back to back on a liquid cold plate. Each plank unit provides a maximum time delay of 600 ps by incorporating a 6-bit TTD core chip at each TRC level to provide a maximum delay of 192 ps in steps of 3.125 ps, and two TTD core chips integrated with 1:4-way PDC level of plank offers a maximum delay of 400 ps, common to four TRCs. The subsequent subsections of this paper delve into

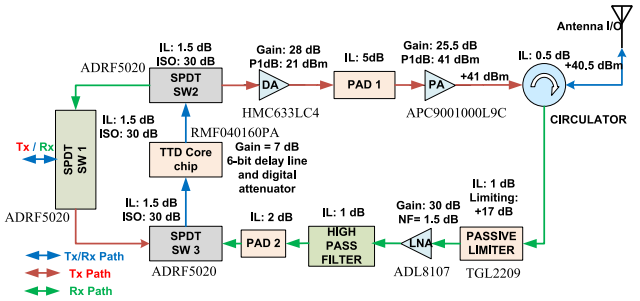

FIGURE 5. Functional block diagram of transmit receive channel.

the design specifics of the major functional blocks within the plank unit.

A. DESIGN OF TRANSMIT-RECEIVE CHANNEL (TRC)

The TRC is the critical functional block of the plank unit and AESA, which is responsible for bi-directional time delay steering, generation of required transmit output power, and low-noise amplification of received signals from the antenna [49], [50]. The design specifications of the X-band TRC given below are derived based on the maximum radar range, scan coverage, and receiver sidelobe level requirement of the AESA imaging radar indicated in section II. The required radar range of 40 Km is achieved by transmit output power of 10W peak at 10% duty, receive noise figure of 4 dB per TR channel [11]. The maximum time delay of 192 ps at the TRC level and 600 ps at the plank level is necessary for scan volume coverage. Further, to achieve receive sidelobe levels better than 25 dB, a time delay resolution of 3.125 ps along with gain control of 31.5 dB in a step of 0.5 dB for Taylor tapering is required [23].

◇ Frequency: 8.5-10.5 GHz

◇ Output Power (Pout): 10W (min.) peak and 1W average power at 10% maximum duty cycle

◇ Switching Time (Tx/Rx): $\leqslant$ 100 ns

◇ Time delay control: 6 bit, 192 ps max delay, 3.125 ps resolution

◇ Rx Gain: 30$\pm$1.5 dB

◇ Rx Gain control: 6 bit, 31.5 dB max attenuation, 0.5 dB resolution

◇ Rx noise figure: 4 dB max.

The functional block diagram of the TRC, as shown in Fig. 5, is designed using COTS RF components. The primary design challenge is fitting RF circuitry within an inter-element spacing of 16 mm while achieving a pulsed output power of 40 dBm (10 Watt) over a 2 GHz bandwidth at X-band. The transmit (Tx) Chain of TRC integrates a cascaded driver amplifier and final GaN power amplifier (PA), which can deliver a minimum pulsed peak power of 12 Watt from APC Technologies. The Receive (Rx) chain of TRC includes a limiter, a low noise amplifier (LNA), and an LTCC high-pass filter (HPF). The circulator, as a duplexer, interfaces both Tx and Rx chains to the antenna in a time-shared manner. For electronic beam scanning and controlling sidelobe levels within the array, the proposed

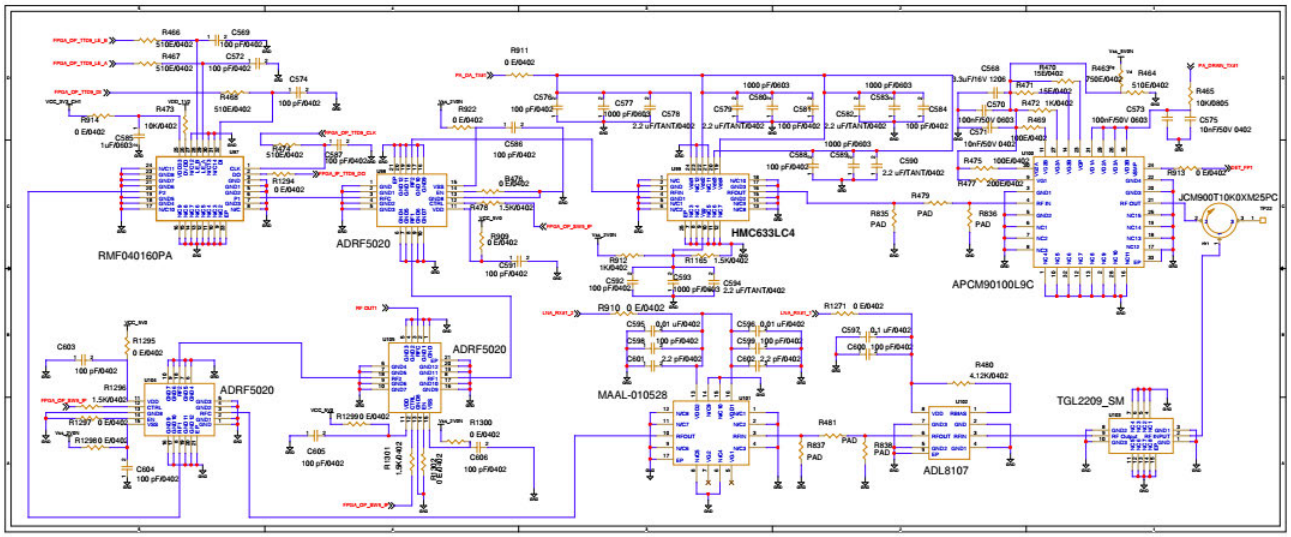

FIGURE 6. Circuit schematic of designed transmit receive channel.

TRC design incorporates a programmable CMOS-based 6-bit TTD line core chip from the RF core, which offers a maximum delay of 192 ps in steps of 3.125 ps. The core chip also integrates a 6-bit digital attenuator, providing a maximum attenuation of 31.5 dB in 0.5 dB steps for sidelobe level control. Chip also integrates gain blocks to provide a gain of 7±2 dB over the bandwidth. The circuit schematic of TRC using COTS components is shown in Fig. 6. The selected core chip only supports unidirectional operation; a separate core chip is required at the Tx and Rx paths, thus increasing the complexity and cost of the system. The design uses three single-pole double-throw (SPDT) switches to convert it into a bi-directional configuration to share a single core chip between the Tx and Rx paths of the TRC. This design optimally utilizes COTS microwave components from Analog Devices, Mini-Circuits, Qorvo, etc., [51], [52], [53], [54], [55] and a TTD core chip in a bi-directional configuration to achieve the desired SWaP performance of the radar system.

B. PLANK CONTROLLER

The plank controller plays a pivotal role and generates precise real-time control and timing signals. It also monitors the operational status of all 16-TRCs. The plank controller is designed using a low-power flash-based SmartFusion2 SOC FPGA from Microsemi to mitigate single-event effects for aerospace systems [56].

This controller interfaces to the system controller via a customised 16-bit asynchronous serial interface at a 10 Mbps data rate over a low-voltage differential signal (LVDS) interface (Serial data input (SDI), Serial data output (SDO)) and timing signals viz., TR pulse (TRP) for Tx/Rx state control, Change of beam (COB), and RESET. To facilitate calibration error data storage, a 64-kilobyte flash memory and Metal Oxide Semiconductor Field Effect Transistor

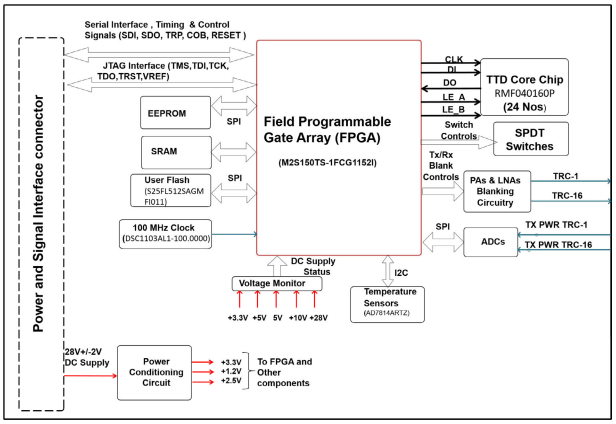

FIGURE 7. Interface diagram of a plank controller.

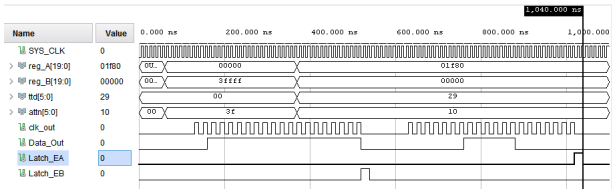

FIGURE 8. Simulated TTD line core chip serial interface timing diagram.

(MOSFET) switches are integrated as blanking circuitry in Tx and Rx paths to reduce power consumption and provide necessary isolation during the calibration of TRCs. It also monitors the Tx power status of 16 TRCs using analog-to-digital converters (ADC), temperature status through the I2C interface, and critical supply voltages. The FPGA interface diagram with different components of the plank unit is shown in Fig. 7. For real-time control of the attenuator and time delay of the TTD line core chip, a five-wire high-speed Serial Port Interface (SPI) viz., Clock (CLK), serial data input (DI),

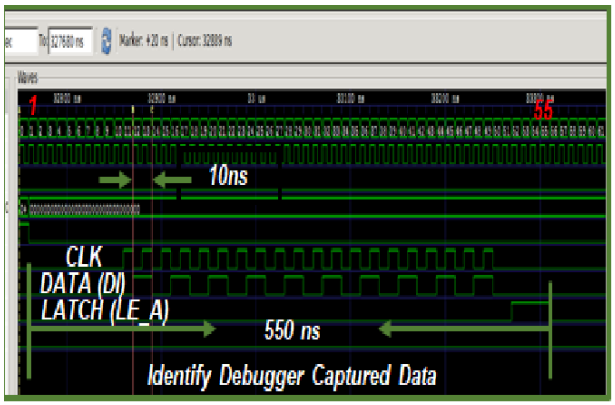

FIGURE 9. Captured TTD line core chip serial interface signals.

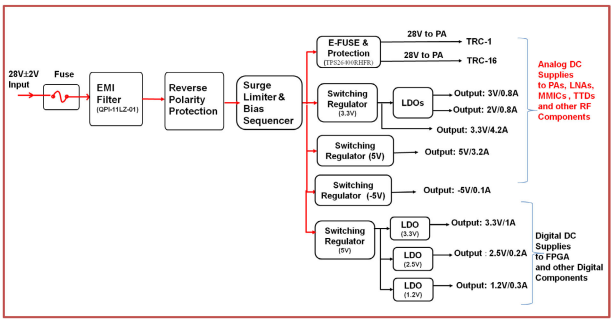

FIGURE 10. Block diagram of plank power supply.

serial data output (DO), latch enable signals (LE_A, LE_B) implemented within the FPGA for each of 24 core chips concurrently at 40 Mbps data rate. Simulated SPI timing diagram of TTD line core chip is shown in Fig. 8. The FPGA also generates the required switch control signals, Tx and Rx blanking control signals to enable and disable selected PAs and LNAs during calibration mode for 16-TRCs. The external clock of 100 MHz is interfaced with FPGA as a master clock for the generation of required internal clock and timing signals. Since more than 300 IO pins are required to provide the above interfaces and to meet the fast beam switching speed of $\leqslant$ 1000μs, all core chips are required to be controlled simultaneously. The captured serial interface timing signals of the TTD line core chip (Clk, Data Input (DI), and Latch (LE_A)) on FPGA using the Inspect debugger tool is shown in Fig. 9. FPGA being a concurrent and event-driven processing machine with more IO intensive, compared to the microcontroller which is a sequential and interrupt-driven processing machine. Hence, FPGA is utilized instead of a microcontroller [57].

C. PLANK POWER SUPPLY

The power supply block of a plank unit consolidates several functions, including EMI filtering, integration of DC-DC converters, switched regulators, and low-dropout (LDO) regulators. It plays a pivotal role in generating the required supply voltages (±5V, 3.3V, 2.5V, 1.2V) for all TRCs and the FPGA controller within the plank unit from a single 28±2V DC supply, as depicted in Fig. 10. Additionally, it incorporates a bias sequencer responsible for sequencing the gate and drain voltages to the MMICs utilized in the TRCs. The power supply block is meticulously designed to provide a low ripple voltage of $\leqslant$10mV with over/under voltage and current protection mechanisms. Furthermore, it includes an automatic thermal shutdown feature, triggered when the temperature exceeds 85^{0}C, ensuring the safety and reliability of the system.

D. DUAL BI-DIRECTIONAL TTD LINE WITH PDC

The plank unit also integrates four COTS 1:4-way Power Divider/Combiners sourced from Mini-Circuits [58] to interface 4 TR channels. These PDCs, in conjunction with dual 6-bit TTD core chips and four SPDT switches, as illustrated in Fig. 11, provide a bi-directional 400 ps maximum time delay common to four TRCs. Furthermore, two COTS 1:2-way PDCs [59] are integrated to provide an RF interface to eight TRCs of plank unit as two quadrant signals in the vertical dimension of the array for implementation of a monopulse receiver channel in elevation. A five-section microstrip BPF is integrated after the 1:2-way PDCs stage to offer the required out-of-band rejection that is common to octal TRCs. The EM simulation plot of dual bi-directional TTD along with 1:4- way PDC is shown in Fig. 12.

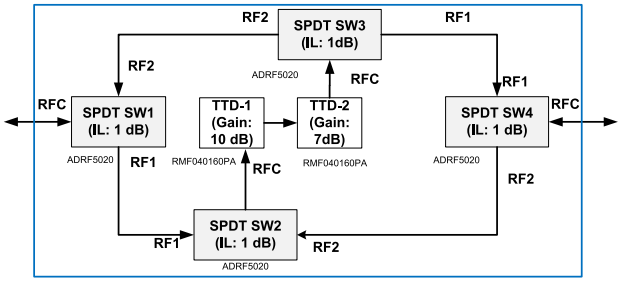

FIGURE 11. Block diagram of Dual bi-directional TTD line.

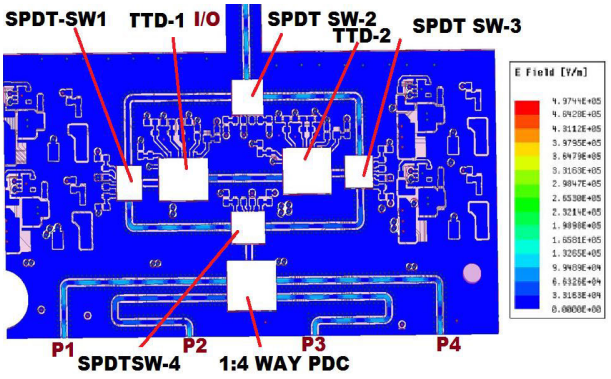

FIGURE 12. EM simulation plot of dual TTD line circuit and PDC.

E. RF PATH SIMULATION OF PLANK UNIT

Prior to the PCB design of the plank, a thorough RF path analysis was carried out by utilizing the selected COTS

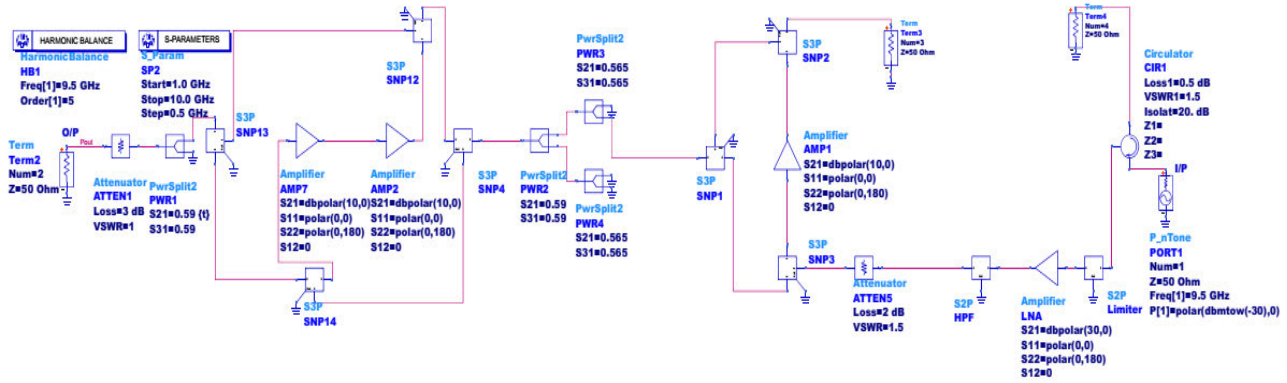

FIGURE 13. Schematic diagram of single TR Channel Receive path simulation.

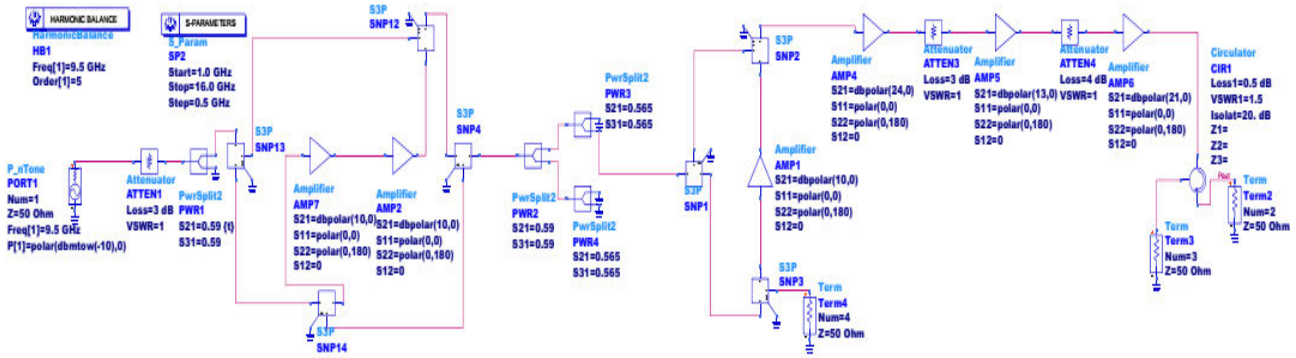

FIGURE 14. Schematic diagram of single TR Channel Transmit path simulation.

components. The main design objective is to generate a minimum peak transmit output power of 40 dBm and achieve a maximum receive noise figure of 4.0 dB per TR channel with a 600 ps maximum time delay over 8.5-10.5 GHz. The design of a single TR channel, both in transmit and receive paths, is simulated using the ADS tool, as shown in Fig. 13 and Fig. 14. The simulated results of cascaded gain at different stages of Rx path with an overall gain of 28.9 dB (without PDC loss) at 9.5 GHz are shown in Fig. 15. The simulated results of cascaded transmit path power at different stages of the TX path, and harmonic levels up to 5^{th} order are shown in Fig. 16 (a) and Fig. 16(b) at 9.5 GHz, depicting transmit output power of $\geqslant$10W, level of even harmonics $\leqslant -40$ dBc and odd harmonics $\leqslant -24$ dBc.

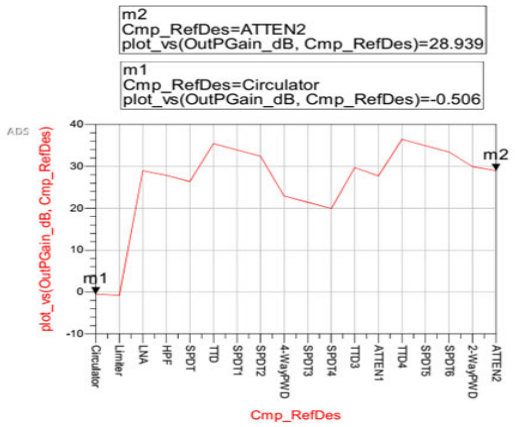

FIGURE 15. Simulated cascaded receive path Gain of single TR Channel at 9.5 GHz.

IV. PLANK PCB AND MECHANICAL DESIGN

The 16-TRCs, along with associated circuits of plank, are meticulously designed on a 14-layer multi-laminate single PCB with dimensions of 290 mm x 190 mm x 2 mm. The RF circuitry within the TR channels and PDCs are engineered on Rogers RO4003C microwave substrate of 8 mils, low loss tangent ($\tan\delta = 0.0027$ @ 10 GHz), and dielectric constant (ϵ_r) of 3.38. Conversely, the plank controller and power supply circuitry were designed using FR4 laminate of dielectric constant (ϵ_r) of 4.17 and thickness of 10 mils. The designed PCB layer stack-up, as shown in Fig. 17, utilizes pre-preg, blind vias, and printed-through holes to create a multi-layer configuration with appropriate inter-layer connections. The designed PCB layer stack-up features a 50Ω impedance for RF lines, incorporating length matching for digital Serial Port Interface lines. This section covers a plank unit's PCB and mechanical and thermal design aspects.

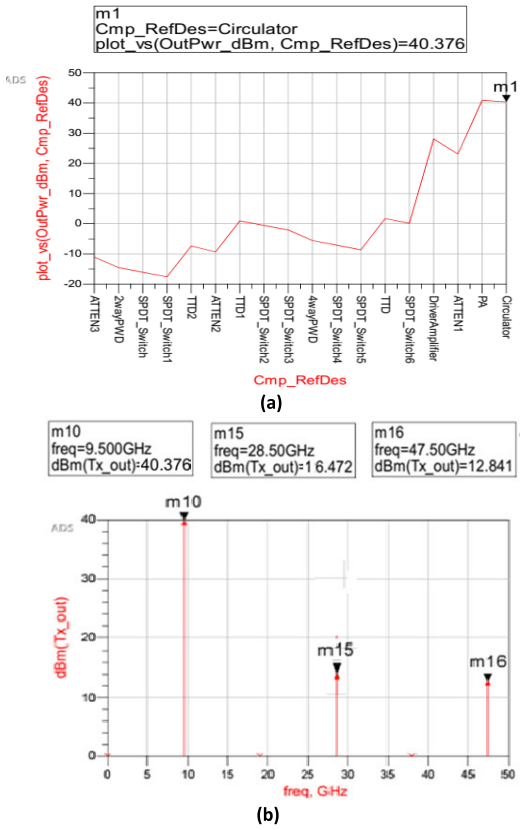

FIGURE 16. Simulated cascaded Transmit path output power and harmonics of single TR Channel at 9.5 GHz: (a) Output Power, and (b) Harmonic levels.

A. PRINTED CIRCUIT BOARD DESIGN

All RF components, including the FPGA and DC-DC converters, are placed on the top layer of the PCB to facilitate ease of debugging and potential rework, except a few passive components of the FPGA controller are placed on the bottom side of the PCB for proper decoupling. The RF circuit layout is meticulously designed and simulated using the ADS software tool. The complete PCB layout, coupled with signal and power integrity analysis for the controller and power supply, is also executed using the Allegro PCB design software tool from Cadence. The PCB layout for all 16-TR channels is identical and optimized to fit within a 15 mm width. To enhance channel-to-channel isolation, narrow partition walls, each of 0.5 mm thickness, are incorporated between adjacent TRCs. Electromagnetic simulations are conducted using the Momentum tool from Keysight to validate the isolation performance and achieve more than 40 dB isolation across the channels and bandwidth. The plank PCB integrates 16 sub-miniature push-on (SMP) connectors for Antenna Input/output (IO), two for RF IOs, and a 30-pin Micro-D connector for signal and power interfaces. Automated surface mount assembly is utilized for component assembly, and the top view of the assembled Plank PCB is illustrated in Fig. 18.

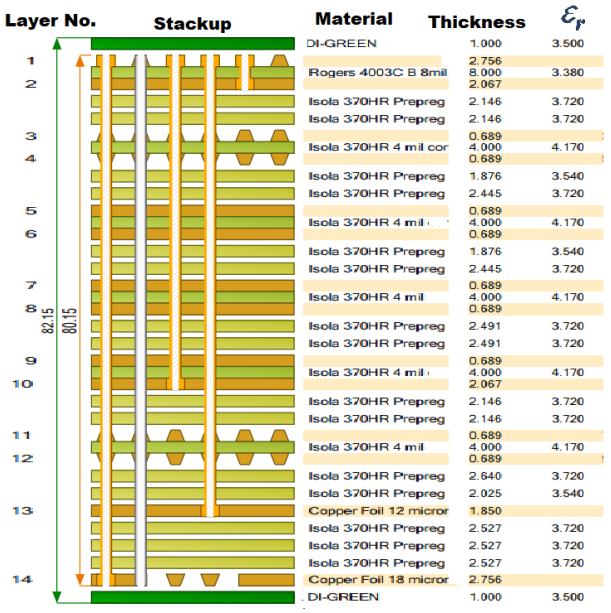

FIGURE 17. Plank PCB layer stack-up.

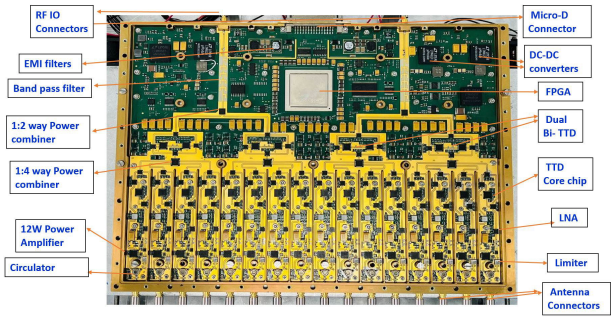

FIGURE 18. Assembled view of designed Plank PCB.

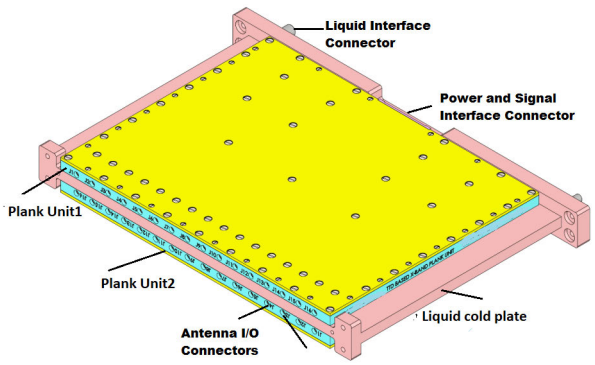

FIGURE 19. Integrated view of two plank units on the liquid cold plate.

B. MECHANICAL AND THERMAL DESIGN

The plank PCB is thoughtfully designed to snugly fit within a mechanical enclosure measuring 300 mm in width, 200 mm in depth, and 8 mm in height. This enclosure for the plank unit is constructed from Wrought Aluminum 6061-T6 material and is yellow-chromated to prevent oxidation. The

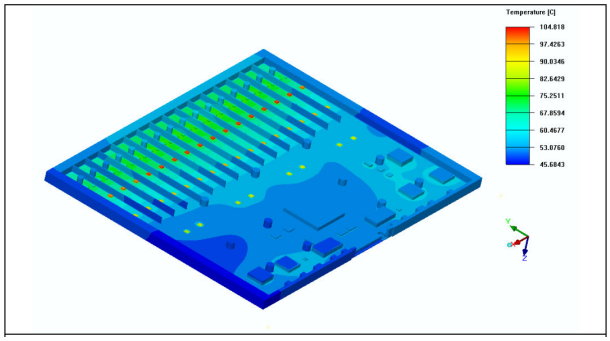

FIGURE 20. Thermal contour plot of plank PCB.

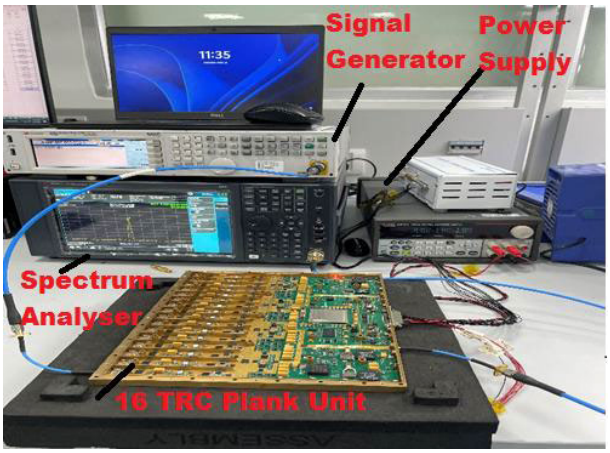

FIGURE 21. Plank unit measurement setup.

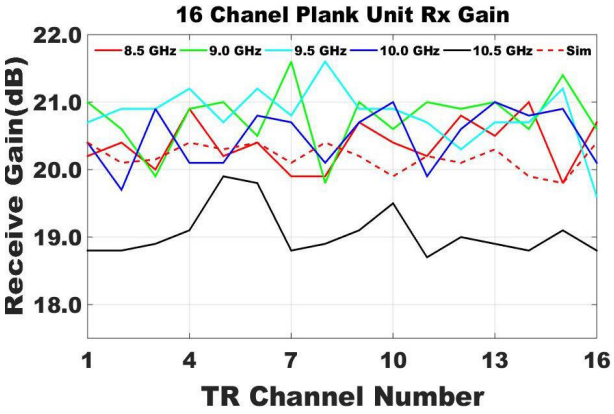

FIGURE 22. Simulated and measured Receive gain of 16- TR Channels.

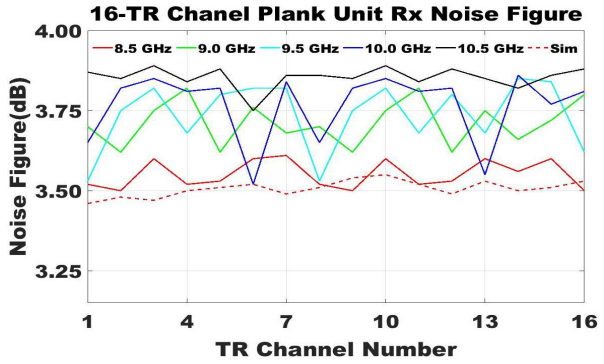

FIGURE 23. Simulated and measured receive noise figure of 16-TR Channels.

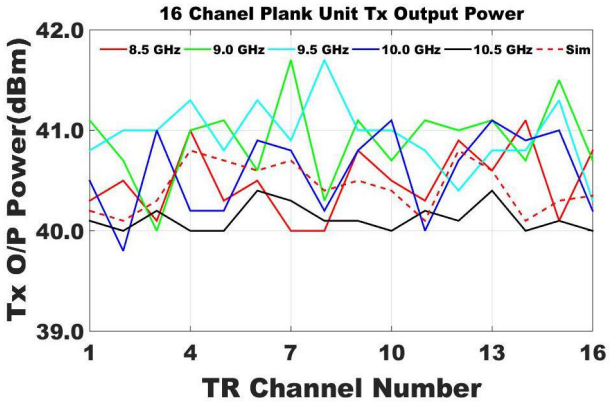

FIGURE 24. Simulated and measured Transmit output power of 16-TR Channels.

TABLE 1. Performance of developed 16-TR channel plank unit.

Parameters	Achieved performance
Frequency	8.5-10.5 GHz
Number of TR Channels	16
Transmit input power	0±1 dBm at RFIO
Transmit peak output power	10 Watt (min) at Antenna IO per TRC
Transmit pulse width and duty	100μs (max) & 10% (max)
Transmit harmonic level	⩽-24 dBc
Receive gain	20±1.5 dB per TRC
Receive Noise Figure	4.0 dB (max)
Rx out of band rejection	⩾40 dBc (⩽7.5 GHz & ⩾12.5 GHz)
Receiver isolation	⩾40 dB
Receiver input damage level	10 Watt (pulsed)
Switching time	100 ns (max)(Time delay, Tx/Rx, attenuator)
Time delay	600 ps(max),3.125 ps resolution
Gain control	31.5 dB (max), 0.5 dB resolution
Power supply and consumption	28±2V DC and 86 Watt
Efficiency and thermal load	19% (min) and 70 Watt (max)
Operating temperature	-40^{0}C to +55^{0}C
Dimension	300 x 200 x 8 mm^3
Weight	1800 grams (max)

plank unit consumes 86 Watt of power (5 Watt per TR channel and 6 Watt consumed by other circuits) at 10% maximum duty cycle operation and delivers an overall efficiency of better than 19%. Two plank units are securely mounted back-to-back on a liquid-cooled plate within the array unit, as depicted in Fig. 19, for effective thermal management. The underside of the plank is firmly affixed to a liquid cold plate, efficiently dissipating the total heat load of 70 Watt. Thermal analysis was meticulously conducted using an 8 mm thick liquid cold plate, fed with a liquid inlet temperature of 45^{0}C and subjected to a maximum ambient temperature of 55^{0}C. The analysis includes the thermal resistance of the mechanical enclosure, PCB, and components, employing a cascaded thermal model for precise evaluation. Fig. 20 displays thermal contour plot of the plank unit, which shows that the hot spot, particularly the final power amplifiers of PCB, is at approximately 105^{0}C. This

TABLE 2. Performance comparison of developed TTD line-based multi-channel TR Modules with relevant works.

Parameters	Current work	[33]	[34]	[40]
Frequency (GHz)	8.5-10.5	16.1-17.3	X-band	1-6
Number of TR channels	16	8	8	8
Architecture	Distributed TTD lines at TRC and PDC	Phase shifter at TRC and TTD lines at PDC	Phase shifter at TRC and TTD lines at PDC	Single TTD line at TRC
PCB	14 layer multi-laminate	LTCC 8 layer multi-laminate	Integrated 3D lead less chip module	8 layer multi-laminate
Transmit Output power (Watt)	10	7	1.5	8 (CW)
Receiver Gain (dB)	21	41	22	15
Receiver Noise figure (dB)	4	3.65	–	6
Time delay (ps)	6-bit, 600 (max), 3.125 step	7-bit, 720 (max),15/60 step	4-bit (0.5λ, 1λ, 2λ, 4 λ)	7-bit, 508 (max), 2/4 step
Dimension (mm^3)	300x200x8	110x65x10	32x20x5	185x155x15
Weight (gms)	1800	65	13	800

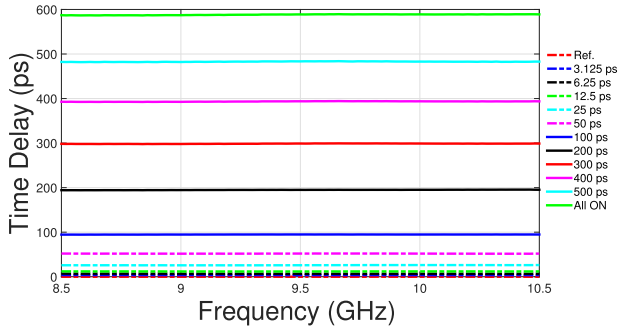

FIGURE 25. Receive path time delay of TR channel-1 over primary states of TTD line.

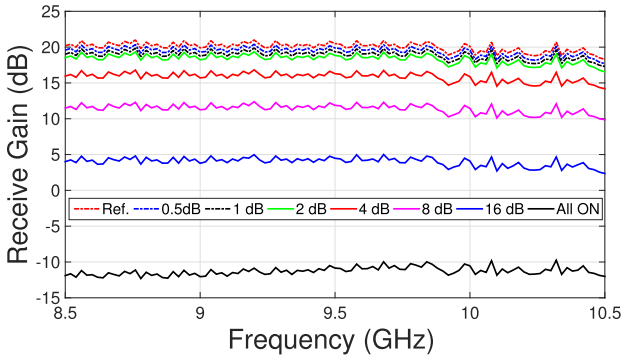

FIGURE 26. Receive Gain of TR channel-1 over primary states of attenuator.

value falls within the Allowable junction temperature range of the components, demonstrating the effectiveness of the plank unit thermal design in maintaining component temperatures within acceptable limits during operation.

V. PERFORMANCE CHARACTERIZATION OF PLANK UNIT

The performance of the developed proto-plank unit is measured in transmit and receive paths of TR channels (Channel 1 to Channel 16) using a Vector Network Analyzer (VNA), Spectrum Analyzer, and Signal Generators from Keysight Technologies. For each of the TRC more than 500 parameters are measured to characterise its performance over different attenuator and time delay states both in Tx and Rx state over full bandwidth. An automated test setup is established by controlling instruments using the Labview tool from National Instruments for performance characterisation of 16-TRCs of plank unit, which reduced the measurement time and improved the repeatability of measurements. The measurement setup is shown in Fig. 21. The performance evaluation of the plank unit is carried out at a liquid inlet temperature of 45^0C over the operating temperature range of -40^0C to $+55^0$C. The measured receive gain, receive noise figure, and transmit output power over for five frequency spots (at 8.5, 9.0, 9.5, 10.0, and 10.5 GHz) along with simulated result at 9.5 GHz for 16-TRCs is shown in Fig. 22, Fig. 23, and Fig. 24 respectively. The measured receiver gain performance is 20 ± 1.5 dB except at 10.5 GHz due to a shift in BPF frequency response, noise figure $\leqslant$3.89 dB, and transmit power is $\geqslant$ 40 dBm across 16-TRCs over 8.5 to 10.5 GHz. Good agreement between simulated and measured results, validate the design of plank across the channels. The receive path time delay and attenuation performance is measured using a VNA across all 64 states of the time delay and attenuator blocks of the TTD line core chip. The time delay is computed from the unwrapped phase data measured using a VNA as per Equation (3).

$$\text{Time delay (ns)} = \frac{\text{U}n - wrapped\ phase\ (Deg)}{360^0 \times \text{F}requency\ (GHz)}. \quad (3)$$

Fig. 25 shows the time delay response for different time delay states, and Fig. 26 presents the receiver gain response for different attenuator states of TRC-1. The measured time delay and gain control is within $\pm5\%$ of the set state value, and no skipping states are observed. The measured results play a pivotal role in validating the plank's overall functionality and performance compliance concerning the overall requirements of AESA. This validation ensures the plank unit is suitable for its intended imaging radar application.

VI. CONCLUSION

This paper presents a novel design of a compact 16-T/R channel X-band plank unit, specifically to provide the large time delay required for squint-free beam steering of a 10 cm resolution imaging radar. The maximum time delay of 1.4 ns in the step of 3.125 ps required for time delay steering of a 512-element AESA is successfully implemented through a distributed time delay network to cover a scan volume of $\pm45^0$ in azimuth and $\pm30^0$ in elevation. This is

accomplished by integrating a 6-bit TTD line core chip in a distributed architecture at both plank unit and quadrant beam former levels. The designed plank unit delivers impressive performance metrics, including a minimum transmit peak output power of 10 Watt, receiver noise figure of 4 dB maximum, and gain of 20 dB including power combiner loss. It exhibits channel-to-channel isolation of better than 40 dB, switching speed of $\leqslant$ 100 ns (time delay, attenuator, TR switch states), and overall efficiency surpassing 19% per TR channel across 2 GHz operating bandwidth and temperature range of -40^0C to $+55^0$C. Remarkably, the 16-TR channel plank unit is ingeniously designed in a compact size, measuring 300 $\times$ 200 x 8 mm^3 and weighing a maximum of 1800 grams. The comprehensive performance summary of the developed plank unit is presented in Table 1. The performance comparison of the developed one with other TTD line based multi-channel TR Modules is given in Table 2. Furthermore, the integration of the current plank design with a 4-16 GHz wideband TTD line core chip in a distributed manner showcases its potential to be utilized in advanced communication, EW, and long-range, high-resolution imaging radar applications across a broader frequency spectrum ranging from 4 to 16 GHz.

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